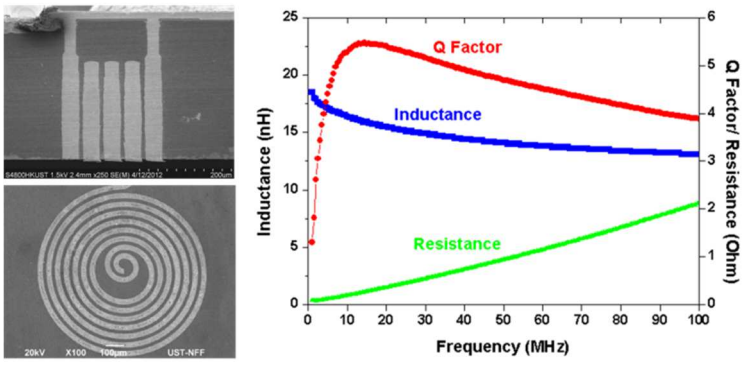
INSTITUT NATIONAL DES SCIENCES APPLIQUÉES CENTRE VAL DE LOIRE

PhD thesis proposal

Passive integration is one of the most important directions in the era of “More than Moore” according to the International Technology Roadmap for Semiconductors (ITRS). After successful integration of resistors and capacitors, integration of magnetic devices with large inductance density, small resistance, and small high-frequency loss is under intensive research. Embedding the magnetic device inside the silicon substrate is an effective approach to implement thick coils for resistance reduction. However, it suffers from more significant high-frequency substrate loss. On the other hand, porous silicon is a promising technique to reduce the high frequency substrate losses [1]. It has been demonstrated for many radiofrequency applications. Therefore, this thesis will introduce porous silicon technology into embedded magnetic devices to achieve excellent magnetic device performance.

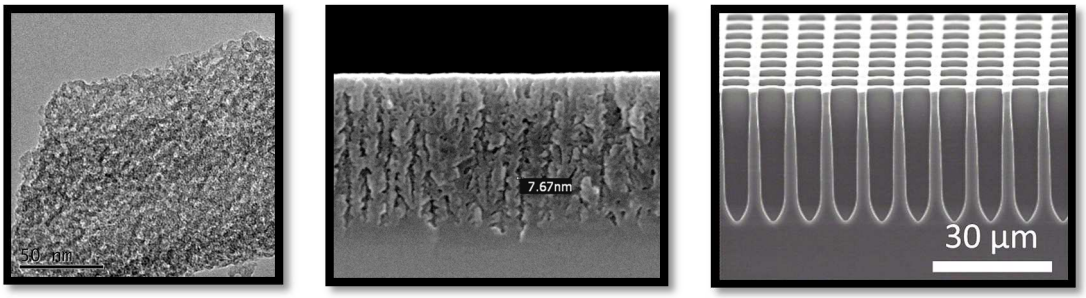
Embedded magnetic devices can effectively utilize the volume of the substrate to achieve better device performance. It can be accommodated in the bottom layer of the substrate and connected to the front-side circuit using vias, so that no extra chip area and profile are needed. For example, Figure 1 shows the photos and the performance of a 0.8 mm^2, 7-turn embedded Cu coil previously characterized. It achieves a large track thickness of 200 um for resistance reduction. It also achieves a high track aspect ratio of around 7:1 and therefore a small track width of 30 um, so that the high frequency eddy current loss is limited and more turns can be realized in a limited area for a large inductance density. The measured performance shows an inductance of 13.1 nH @ 100 MHz, a DC resistance of 49 mΩ, and a peak Q_factor of 5.5 @ 16 MHz (substrate resistivity 8 Ω-cm) [2]. It can be seen that the L/R_{DC} of 0.27nH/mΩ is quite good considering no magnetic core is applied. However, the Q is relatively low due to the significant capacitive substrate losses since the coil has a large overlap area with the substrate at the track sidewalls. Knowing that the dielectric permittivity and the resistivity is lower in the case of PS, the use of such material between the coils is a promising alternative. This perspective was already demonstrated by simulation [3].



a) b)

Fig. 1 (a) SEM images of embedded Cu coil (upper: cross-sectional view of a testing structure, lower: bottom view of the coil) (b) L, R, Q vs. f of the embedded Cu coil [2].

Porous silicon is formed by electrochemical etching (anodic dissolution) of crystalline silicon wafers in hydrofluoric acid based electrolytes. According to the substrate doping, the crystalline orientation, the electrolyte composition and temperature or the anodization conditions (applied current, duration, etc…), various morphologies can be achieved. The pore dimensions vary from a few nanometers to several micrometers (Figure 2).



a) b) c)

Fig. 2 (a) TEM picture of microporous silicon with average pore diameters around 2 nm. (b) SEM picture of a mesoporous silicon layer cross section. (c) SEM picture of a macropore array.

Since 2003, the GREMAN seeks to develop new applications of this material in microelectronics devices or energy micro-sources. In particular, the current objectives of its work on Microelectronics devices include the electrical isolation under RF devices (inductances, filters…) at high frequencies, the electrical isolation around AC switches (TRIACs for instance), the development of anisotropic structures by electrochemical etching for 3D devices (conducting via, capacitors…) and the electrochemical etching of wide band gap semi-conductors (GaN, SiC, ZnO) for power devices or energy harvesting. Some applications in energy micro-sources are also studied such as PS hydrogen diffusion layers for Proton Exchange Membrane micro Fuel Cells (PEMFC) or Si nanowires, porous silicon nanoparticles and PS for Lithium Micro-batteries.

For RF applications, the substrate must be as resistive as possible and its dielectric permittivity must be lowered in order to reduce current losses and capacitive couplings. For this purpose, glass is a widely used substrate. Nevertheless, it cannot allow any heterogeneous integration of both active and passive devices. As a consequence, porous silicon is a promising candidate as we can localize the resistive regions under the device area [4,5]. In order to evaluate the interest of porous silicon (PS) substrates regarding to reference substrates (glass and silicon), lumped devices (inductors and transmission lines) were integrated on PS and characterized [6,7,8]. The use of PS was found to increase drastically the performance of these planar devices.

PS can also be fabricated locally on the silicon substrate to form a silicon / PS hybrid substrate. The latter is an interesting alternative to the silicon substrate for monolithic integration of RF circuits. Indeed, while active devices are integrated on silicon, passive devices are integrated on the PS regions. To demonstrate the feasibility and the impact of the hybrid substrate, we integrated and characterized radiofrequency circuits. The prototypes were composed of filter and ESD protection diodes commercialized by STMicroelectronics (Figure 3) [9,10].

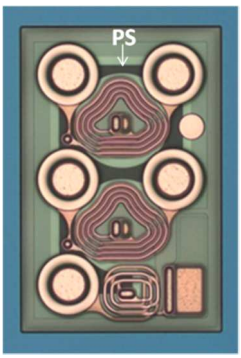


Fig. 3. RF circuit prototypes integrated on silicon / PS hybrid substrates (Common mode filter and ESD protection diode).

During this thesis, the electrochemical etching of PS on trench walls will be firstly studied. This work will lead to the determination of the optimal PS thickness and morphology to obtain high isolation performances. Then, specific structures will be designed in order to integrate magnetic materials in the device. Two different strategies could be employed. PS can be functionalized by magnetic material impregnation or the magnetic layers can be deposited on one side of the wafer.

During this work, the equipments of the CERTeM (Centre d'Etude et de Recherche en Technologie Microélectronique) platform in Tours will be used. A 450 m² cleanroom class 100, benefiting of ST infrastructure, regroups many equipments dedicated to photolithography, etching, deposition or cleaning. In addition, many means of characterization are available (ellipsometry, microscopy, electrical measurements, RX diffraction, FTIR, Raman, etc…).

The main supervisor in INSA-CVL will be Pr. Gael Gautier. Dr Jérôme Billoué (University of Tours) will be co-supervisor of this thesis.

Website: greman.univ-tours.fr

References

[1] G .Gautier and P. Leduc, “Porous silicon for electrical isolation in RF devices: A review”, Applied Physics Reviews, vol. 1, 011101, 2014.

[2] R. Wu, J. K. Sin and C.P. Yue, “High-Q Backside Silicon-Embedded Inductor for Power Applications in µH and MHz Range”, IEEE Transactions on Electron Devices, vol. 60(1), pp. 339-345, 2013.

[3] J. Zhou, R. Wu, J. Billoué, G. Gautier, “Backside Silicon-Embedded Inductor Using Porous Silicon Layer for Substrate Effect Suppression”, Conférence IEEE EDSSC, Chengdu (Chine), Juin 2014.

[4] S. Ménard, A. Fèvre, J. Billoué and G. Gautier, “P type porous silicon resisitivity and carrier transport”, Journal of Applied Physics, vol. 118, 105703, 2015.

[5] M. Capelle, J. Billoué, G. Gautier and P. Poveda, “RF performances of inductors integrated on localised p-type porous silicon regions”, Nanoscale Research Lett., vol. 7, pp. 523-530, 2012.

[6] J. Billoué, G. Gautier and L. Ventura, “Integration of RF inductors and filters on mesoporous silicon isolation layers”, Phys. Stat. Sol.(a), vol. 208, No 6, pp. 1449-1452, 2011.

[7] M. Capelle, J. Billoué, P. Poveda and G. Gautier, “N-Type Porous Silicon Substrates for Integrated RF Inductors”, IEEE Trans. On Electron Devices, vol. 58, No. 11, pp. 4111 – 4114, 2011.

[8] M. Capelle, J. Billoué, P. Poveda, G. Gautier, “Study of porous silicon substrates for the monolithic integration of radiofrequency circuits”, International Int. Journal of Microwave and wireless technologies 2014.

[9] M. Capelle, J. Billoué, J. Concord, P. Povéda, and G. Gautier, “Monolithic integration of low-pass filters with ESD protections on silicon/porous silicon substrates”, Solid-State Electronics, vol. 116, pp. 12-14, 2016.

[10] M. Capelle, J. Billoué, P. Poveda, and G. Gautier, “Porous Silicon/Silicon Hybrid Substrate Applied to the Monolithic Integration of Common-Mode and Bandpass RF Filters”, IEEE Trans. on Electron Dev., vol. 62, No 12, pp. 4169-4173, 2015.